AMENDMENTS TO THE SPECIFICATION

IN THE TITLE:

Please amend the title as follows:

~~VERTICAL~~ FLOATING GATE TRANSISTOR WITH HORIZONTAL GATE LAYERS STACKED NEXT TO VERTICAL BODY

IN THE SPECIFICATION:

Please replace the paragraph beginning at page 9, line 26, with the following rewritten paragraph:

In a similar manner, the second array 170 includes transistors 200 arranged in cells 215AA, 215AB...215AN in a first dimension, e.g., in the X-dimension of the second array input lines OL1-OLN, and in cells 215AA, 215BA...215NA in a second dimension, e.g., in the Y-dimension of second array output lines B1-BN 224. Each of the logic cells 215 thus includes a transistor 200 having a floating gate 202 and one of the first array output lines OL1-OLN. The first array output lines OL1-OLN serve as the second array input lines OL1-OLN. The second array input lines OL1-OLN are also referred to as second control lines 220. Because of the substantially identical nature of logic cells 205 and 215, only logic cells 205 are discussed in detail in the following paragraphs.

Please replace the paragraph beginning at page 11, line 25, with the following rewritten paragraph:

Figure 5 is a schematic diagram illustrating one embodiment of a programmable decoder array 116, e.g., the X gate decoder 115. The architecture of the other programmable decoders 120, 125 is substantially similar and is not discussed in detail. The programmable decoder array 116 of Figure 5 is implemented with a plurality of transistors 200, each having a corresponding floating gate 202. The floating gates 202 control electrical conduction between the sources S1-SN and drains 242.

Please replace the paragraph beginning at page 12, line 26, with the following rewritten paragraph:

Figures 7A and 7B illustrate a top view and a front view, respectively, of a portion of an array having split control gates, i.e. two adjacent control gates 335. In the embodiment shown in Figures 7A and 7B, the two control gates 335 overlaying corresponding floating gates 202 are next to each other, as illustrated by logic cells 205AA, 205AB, 205BA and 205BB. Figure 7A illustrates, by way of example, the output lines OL1 and OL2, which are shown schematically for clarity. In one embodiment, the control gates 335 are coupled to the control lines C1-CN 210 of the FPLA 141. One advantage of the split control gates 335 is that only one transistor 200 is required per logic cell 205. Each of the transistors 200 can be individually selected when the split control gates 335 are isolated from each other.

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Please replace the paragraph beginning at page 18, line 8, with the following rewritten paragraph:

Figure 12 is a perspective view of another embodiment of vertical transistors with horizontal gate layers, illustrated by a portion of an array having a single control gate (e.g., XG2) 335 overlaying split floating gates 202. For example, the embodiment of Figure 12 is a portion of the completed memory cell array 106, including four logic cells 265AA, 265AB, 265 BA and 265BB.

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